REMARKS

Claims 1-3, 5, and 11-17 are pending in the instant application. In view of the following remarks, reconsideration of the instant application is respectfully requested.

The Examiner has still not acknowledged the claim of priority and receipt of the priority documents in the present application, which were submitted with the original application on October 29, 2003. Applicants again respectfully request acknowledgement of the priority claim and the submission in the next Office communication.

Claims 1, 5, 11-13, and 16 are rejected under 35 U.S.C. 102(b) as being unpatentable over United States Patent No. 5,156,989 to Williams et al. (hereinafter referred to as Williams). Applicants respectfully traverse.

Claim 1 relates to a semiconductor integrated circuit that includes, inter alia, a ***silicon substrate*** and a ***silicon epitaxial layer that touches the surface of said silicon substrate and has a lower resistivity than the resistivity of said silicon substrate***. The semiconductor integrated circuit of claim 1 also includes first and second circuit sections formed in said silicon epitaxial layer and a device isolation region projecting from said silicon substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections.

The Office Action asserts that figure 25P of Williams discloses the structure of claim 1. Specifically, the Office Action asserts that element 111 discloses a silicon substrate, element 121 discloses a silicon epitaxial layer, and the sections on both sides of the ISO region disclose first and second circuit sections. The Office Action asserts that element 129a of Williams apparently illustrates an isolation zone that extends to the surface of the substrate. The Office Action asserts that Williams discloses the epitaxial layer having a lower resistivity than the substrate at col. 10,

lines 54-55, which indicates that "the p substrate 111 may be doped lighter than the p epitaxial layer 121 (Office Action; page 2, lines 11-12).

However, Williams does not identically disclose the feature of claim 1 of first and second circuits being formed in said second epitaxial layer. Since the circuit in figure 25P of Williams on the right side of ISO region 129a is apparently in layer ***121e***, and not in layer ***121***, it does not appear that this circuit is in ***an epitaxial layer touching the silicon substrate***. The description in Williams describes layer 121e as being "enclosed" and "bounded below by an n or n+ buried layer 123 ... and on each of two or more sides by a substantially annular n+ up-isolation region 125 and a substantially annular down-isolation region 129 ... that overlap the buried layer 123 at the edges thereof." (Williams; col. 9, lines 63-70). In Williams, layer 121e does not touch silicon substrate 111, but rather appears to contact N+ buried layer 123. Therefore, it does not appear that both circuits reside in a common epitaxial layer in which the epitaxial layer touches the surface of the silicon substrate. Since Williams does not identically disclose the features of claim 1, Williams does not anticipate claim 1.

Claims 5, 11-13, and 16 ultimately depend from claim 1 and are therefore allowable for at least the same reasons as claim 1 is allowable.

Claims 2, 3, 14, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams. Applicants respectfully traverse.

Claims 2, 3, 14, 15, and 17 ultimately depend from claim 1 and are therefore allowable for at least the same reasons as claim 1 is allowable.

Additionally, the feature of claim 2 that the resistivity of said silicon substrate is between 20 and 100 times the resistivity of said silicon epitaxial layer is independently allowable. The modification of the reference is improperly based on hindsight reasoning and, contrary to the

statement in the Office Action, the particular resistivity has the advantage recited in the specification discussed in the specification at page 6, lines 11-15. The Examiner asserts that such a feature would have been obvious and within the ability of one skilled in the art. (Office Action; page 3, section 3). However, the particular resistivity of the present invention as recited in claim 2 has the advantage recited in the specification, and presented in the previous amendment, that:

> noise electric current flowing in the support substrate is effectively inhibited while the resistivity of the semiconductor layer is maintained in a range where the platform of the conventional device process can be used.

(Specification; page 6, lines 11-15). This effect is also shown in figure 4 of the present application. Williams does not disclose the lower resistivity in the epitaxial layer with respect to the silicon substrate, and the particular resistivity has the specific advantage recited in the specification quoted above. Therefore, the modification of Williams asserted in the Office Action in the rejection of claim 2 results from improper hindsight reasoning.

Claim 3 depends from claim 2 and is therefore allowable for at least the same reasons as claim 2 is allowable.

CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,

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